

REMARKS

The present Amendment amends claims 1-4, 6-11, 13 and 14 and leaves claims 5 and 12 unchanged. Therefore, the present application has pending claims 1-14.

Applicants' Attorney, the undersigned, and Applicants' Japanese Representative Mr. Hiroshi Kawano wish to thank Examiner Matthew Bradley and Supervisory Patent Examiner Donald Sparks for the courtesy extended during the interview of December 9, 2005. During such interview, an agreement was reached that Matsunami appears to have been overcome by the proposed amendments presented during the interview.

During the interview, it was shown that the present invention, contrary to that taught by Matsunami, teaches a channel controller 110 as illustrated in Fig. 1 which is connected between the LAN 400 and the data transfer network 150 so as to conduct the transfer of data from an information processing device 200 connected to the LAN 400 and a storage volume 310 connected to a disk controller 140 which is connected to the data transfer network 150.

According to the present invention as now more clearly recited in the claims and as illustrated, for example, in Figs. 1 and 7, the data transfer network 150 is provided so as to interconnect the channel controllers 110, the disk controllers 140 and a first memory 130 to each other.

Further, unique according to the present invention as discussed during the interview is that the channel controller 110 has an internal structure such as that illustrated in Fig. 7. The channel controller 110 as illustrated in Fig. 7 is intended to

transfer file system type data from the information processing device 200, convert the file system type data to block data and store the block data at the first memory. Also, unique according to the present invention is that a data transfer device 114 is provided so as to allow for high speed transfer of data between the information processing device 200 and the first memory 130.

As discussed during the interview, the above is accomplished by providing as recited in the claims, and as illustrated in Fig. 7, that the channel controller 110 is equipped with a first processor 119 for outputting a block basis I/O request corresponding to the data input/output request and controlling the first memory 130, a file access circuit which has a second processor 112 and a second memory 113 controlled by the second processor 112 and serves to control the transmission/reception of the data input/output request and the data sent from the information processing device 200, a data transfer device 114 for controlling data transfer between the first memory 130 and the second memory 113, and a third memory 117 controlled by the first processor 119. The second processor 112 transmits information indicating the storage position of the data in the second memory 113 to the first processor 119 and the first processor 119 writes into the third memory 117 data transfer information containing information indicating the storage position of the data in the first memory 130 and information indicating the storage position of the data in the second memory 113 and the data transfer device reads out the data transfer information from the third memory 117 and controls data transfer between the first memory 130 and the second memory 113 based on the data transfer information thus read out.

The above described features of the present invention clearly recited in the claims are not taught or suggested by Matsunami whether taken individually or in combination with any of the other references of record.

As discussed during the interview, Matsunami teaches a file server 30 which corresponds to the channel controller as recited in the claims. The contents of the file server 30 as taught by Matsunami is illustrated in Fig. 4. As discussing during the interview, the internal structure of the file server 30 as taught by Matsunami is entirely different from that of the present invention as recited in the claims. Particularly, Matsunami does not teach or suggest that the file server 30 includes first and second processors as recited in the claims each performing different functions. The first processor according to the present invention outputs a block basis I/O request and controls the first memory whereas the second processor controls the second memory and controls the transmission/reception of the data input/output request and the data sent from the information processing device. Such features are clearly not taught or suggested by Matsunami.

Further, as discussed during the interview, there is no teaching or suggestion in Matsunami of a data transfer device such as that recited in the claims. Matsunami teaches a data transfer controller 305 but such data transfer controller simply controls the transfer of data between the communication controller 309 and the fiber channel controller 304. There is no such teaching or suggestion at any point in Matsunami that a third memory is provided within which position information is stored by the first and second processors so as to permit the data transfer device to retrieve such position information and access the data to be transferred between the first

memory and the second memory based on such position information as in the present invention as recited in the claims.

Thus, as agreed during the interview, the present invention since it incorporates the proposed amendments to the claims overcomes the Matsunami and thereby overcomes the 35 USC §102(a) and 35 USC §102(e) rejections of the claims based on Matsunami. Accordingly, reconsideration and withdrawal of these rejections of claims 1-4 is respectfully requested.


The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-14.

In view of the foregoing amendments and remarks, applicants submit that claims 1-14 are in condition for allowance. Accordingly, early allowance of claims 1-14 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (TMI-128).

Respectfully submitted,

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